30. The device of claim 29 wherein the semiconductor region includes an upper region of a first conductivity type; a middle region of a second conductivity type, opposite to the first conductivity type; and a lower region of the first conductivity type, the middle region being positioned between the upper and lower regions such that a transistor is formed that includes the conductive filler as a gate, the upper region as a first source/drain, and the lower region as a second source/drain.

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REMARKS

Claims 1-7 and 20-30 will be pending upon entry of the present amendment. Claims 8-19 are being canceled. Claims 29-30 are being newly presented. The applicant hereby affirms the election of claims 1-7 and 20-28.

The applicants appreciate the acknowledgement of the claim for foreign priority. The certified copy of Italian application TO99A 001086, from which this application claims priority, is enclosed herewith.

Claims 1-7 20-23, and 26-28 were rejected under 35 U.S.C. § 102(b) as being anticipated by Japanese patent publication JP 61-232657 to Sakai et al. ("Sakai").

Sakai does not disclose the invention recited in claim 1. Claim 1 recites an integrated device that includes a high-voltage resistor with a vertical current flow structure. Sakai does not disclose such a resistor with a vertical current flow structure. Instead, Sakai shows a resistor R with a horizontal current flow structure. As can be seen in Figure 1 of Sakai, the resistor R is a rectangle that extends lengthwise across the surface of the device and has two small, square contacts also on the surface of the device. As such, the current flow of the resistor R will be horizontal, and along the surface of the device between the square contacts.

Further proof that the current flow of the resistor R will not be vertical can be found in Figure 2 of Sakai. Figure 2 shows an "n" region under the resistor R and above a P-doped substrate 1, thereby forming a PN junction under the resistor R. As is well known in the art, such a PN junction will prevent current in the resistor R from flowing vertically toward the

PN junction. Thus, the resistor R has only a horizontal current flow structure, and not the vertical current flow structure recited in claim 1.

For the foregoing reasons, claim 1 is not anticipated by Sakai. Claims 2-7 depend on claim 1, and thus, also are not anticipated by Sakai.

Although the language of claims 20-28 is not identical to that of claim 1, the allowability of claims 20-28 will be apparent in view of the above remarks. In particular, claim 20 recites a device with a resistor that extends longitudinally into a semiconductor body. As discussed above, the resistor R of Sakai extends longitudinally along the surface of the device rather than into a semiconductor body. Accordingly, claims 20-28 are not anticipated by Sakai.

Claims 24-25 were rejected under 35 U.S.C. § 103 as being unpatentable over Sakai in view of U.S. Patent No. 5,229,310 to Sivan.

Sakai and Sivan do not teach or suggest the invention recited in claims 24-25. In particular, like Sakai, Sivan does not suggest a resistor formed by a doped semiconductor region extending longitudinally into a semiconductor body. Instead, Sivan refers to a vertically oriented thin-film transistor.

Claim 25 further recites that the device includes a transistor having a gate formed by a conductive filler positioned within insulating walls of the insulating region, a first source/drain formed by an upper region of a semiconductor region that is laterally surrounded by the insulating region, and a second source/drain formed by a lower region of the semiconductor region. Sakai and Sivan do not teach or suggest such a transistor structure. Instead, Sakai shows a bipolar transistor having no gate and no source/drain regions. Sivan shows a transistor with a gate 38 formed in a trench 18 and a first electrode 26 formed under the gate 38 in the trench 18. Such a first electrode 26 cannot possibly be either of the first and second source/drain regions recited in claim 25 because the first electrode 26 is not part of a semiconductor region that is laterally surrounded by an insulating region.

The applicant submits that the only way to arrive at the claimed invention from Sakai and Sivan is to improperly pick and choose from those references using the applicant's disclosure as a template. Nothing in either reference suggests a reason to, or how to, convert the bipolar transistor of Sakai to the field effect transistor of Sivan. Moreover, nothing in either reference suggests taking only the portion of Sivan related to the conductive gate 38 being

surrounded by an insulating layer 32 without also positioning the first and second electrodes 26, 28 outside of the insulating layer 32. As discussed above, the first and second source/drain regions of claim 25 are part of a semiconductor region that is surrounded by the insulating region – not outside of the insulating layer 32 as in Sivan.

For the foregoing reasons, claims 24-25 are nonobvious in view of Sakai and Sivan.

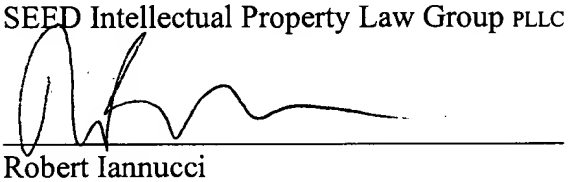
The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Davide Patti

SEED Intellectual Property Law Group PLLC



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